REMARKS

Claims 1 - 26 are pending in the present application. No amendment is presently being made.

Applicant notes that section 5 of the Office Action indicates that claims 10 – 16 would be allowable if rewritten in independent form. However, as explained below, Applicant believes that all of the claims are presently in condition for allowance, and as such, there is no need to rewrite any of claims 10 – 16.

In section 2 of the Office Action, claims 1 – 9, 17 – 19 and 23 – 26 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,353,377 to Parks (hereinafter "the Parks patent"). Applicant is traversing this rejection.

Claim 1 provides an apparatus for supplying a plurality of clock signals. The apparatus includes, *inter alia*, a superperiod signal generating unit for deriving, from a dedicated clock signal of a set of clock signals, a first superperiod signal having a signal period that is a common multiple of the clock signals' signal periods.

The Parks patent discloses an apparatus for synchronizing signals operating at different clock speeds (Abstract). In this regard, the Park patent, with reference to FIG. 2, discloses signal synchronization logic 200 that includes phase locked loop (PLL) clock generator logic 202 (col. 5, lines 12 – 13). As stated at col. 5, lines 14 – 16:

> The PLL clock generator logic 202 multiplies the frequency of the faster clock signal up to the least common multiple of the two frequencies to generate a base clock signal. (emphasis added)

FIG. 3 is a timing diagram that shows two clocks of different speeds (i.e., slow clock and fast clock), and the base clock signal. As is clear from FIG. 3, the base clock has a period that is significantly less than that of either of the slow clock or the fast clock. This is because, as implied by the passage at col. 5, lines 14 – 16, the frequency of the base clock is the least common multiple of the slow clock and fast clock frequencies.

The Office Action suggests that the base clock of the Parks patent is similar to the first superperiod signal of claim 1. Applicant respectfully disagrees.

In the Parks patent, since the base clock has a frequency that is the least common multiple of the slow clock and fast clock frequencies, the base clock has a period that is significantly less than that of either of the slow clock or the fast clock, and therefore the period of the base clock is not a common multiple of the slow and fast clock periods. That is, the Parks patent discloses a common multiple of clock frequencies, not a common multiple of clock periods. Thus, the Parks patent does not disclose a superperiod signal generating unit for deriving, from a dedicated clock signal of a set of clock signals, a first superperiod signal having a signal **period** that is a common multiple of the clock signals' signal **periods**, as recited in claim 1. Hence, the Parks patent does not anticipate claim 1.

Claims 23, 24 and 26 are independent claims, and each includes a recital similar to that of claim 1, as described above. Accordingly, for reasoning similar to that provided in support of claim 1, the Parks patent does not anticipate any of claims 23, 24 or 26.

Claims 2 – 9, 17 and 18 depend from claim 1, and claim 25 depends from claim 24. By virtue of these dependencies, claims 2 – 9, 17, 18 and 25 are all novel over the Parks patent.

Applicant respectfully requests reconsideration and withdrawal of the section 102(b) rejection of claims 1 – 9, 17, 18 and 23 – 26.

In section 4 of the Office Action, claims 20 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Parks patent in view of U.S. Patent No. 6,754,868 to Bristow et al. (hereinafter "the Bristow et al. patent). Applicant is traversing this rejection.

Claim 20 – 22 depend from claim 1. As explained above, the Parks patent does not disclose all of the elements of claim 1. The Bristow et al. patent does not make up for the deficiencies of the Parks patent as the Parks patent relates to claim 1. Accordingly, Applicant submits claim 1, and by virtue of

their dependencies, claims 20 –22, are all patentable over the cited combination of the Parks and Bristow et al. patents.

Applicant respectfully requests reconsideration and withdrawal of the section 103(a) rejection of claims 20 – 22.

Section 7 of the Office Action includes a response to arguments that Applicant presented in an amendment that Applicant mailed on 3 OCT 2005. In the response, the Office Action quotes a passage from Applicant's arguments, and emphasizes that a least common multiple is a subset of a common multiple. However, Applicant's argument was not directed toward a relationship between a common multiple and a least common multiple, but instead, between frequencies and periods. Thus, Applicant is standing by Applicant's assertion that in the Parks patent, since the base clock has a frequency that is the least common multiple of the slow clock and fast clock frequencies, the base clock has a period that is significantly less than that of either of the slow clock or the fast clock, and therefore the period of the base clock is not a common multiple of the slow and fast clock periods.

In view of the foregoing, Applicant respectfully submits that all claims presented in this application patentably distinguish over the prior art. Accordingly, Applicant respectfully requests favorable consideration and that this application be passed to allowance.

Respectfully submitted,

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Date

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